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EP 0107902 A2 EP 0072966 A2 EP 0020994 A1
WO 87/04856 A1

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(71) Applicant
Samsung Electronics Company Limited

(Incorporated in the Republic of Korea)

416 Maetan-dong, Kwonsun-gu, Suwon-city, Kyounggi-do, Republic of Korea

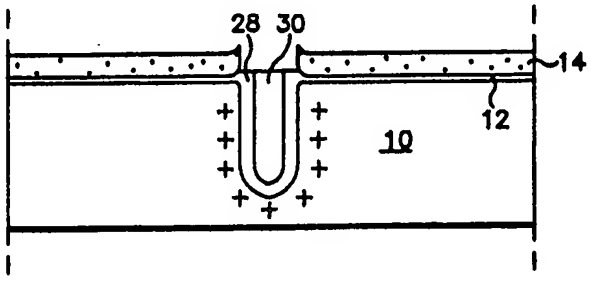
(72) Inventors
Hyeon-Jin Cho
Soo-Gil Yang

(74) Agent and/or Address for Service
Appleyard Lees
15 Clare Road, Halifax, West Yorkshire, HX1 2HY, United Kingdom

(54) Element-isolating process for a semiconductor device

(57) A process for forming isolation trenches for a semiconductor device includes the steps of: etching a part of a first conductive layer corresponding to the trench region, and thermally oxidizing the remainder of the first conductive layer, to form an oxidized first conductive layer; removing a portion of a second 14 and first 12 insulating layer formed over the substrate, by using the oxidized first conductive layer as a mask, and thereafter etching the exposed substrate, to form a trench; depositing a buffer oxide layer and a second conductive layer of polycrystalline silicon on the inner wall of the trench and above the insulating layers respectively; and filling the interior of trench with only the oxidised second conductive layer 28 or additionally with an insulating material 30 other than a nitride layer. Thus the trench may have a width smaller than that obtained by photo-etching techniques. Further, because the interior of trench may be filled with only oxidised polycrystalline silicon the trench may have a width of 0.3μm - 0.4μm without bird's beak phenomenon.

FIG. 2I



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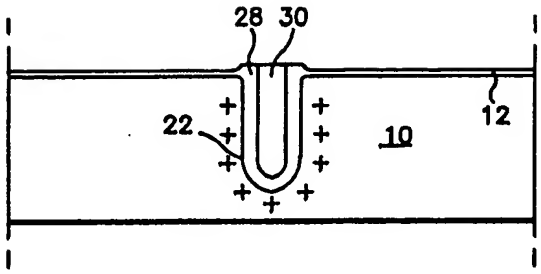


FIG. 1

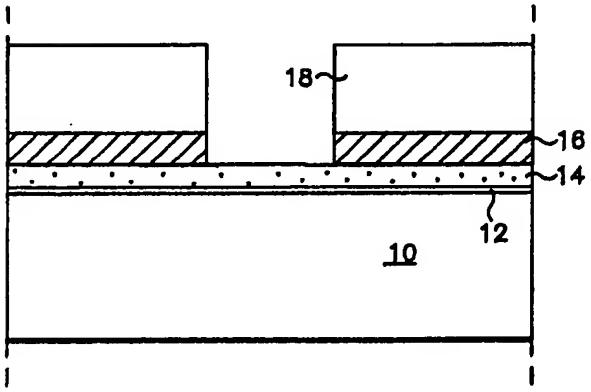


FIG. 2A

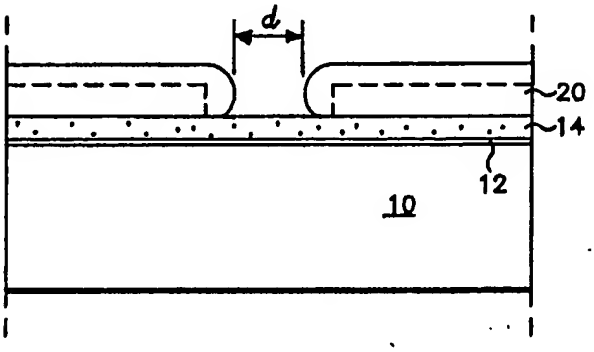


FIG. 2B

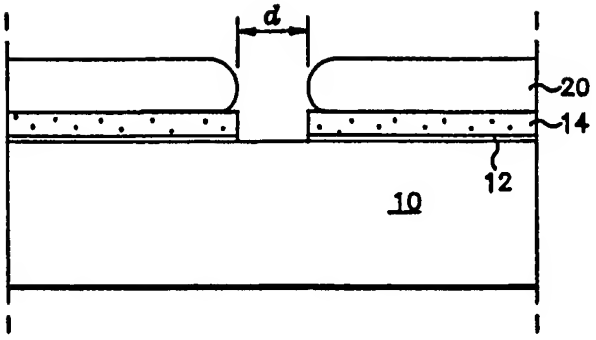


FIG. 2C

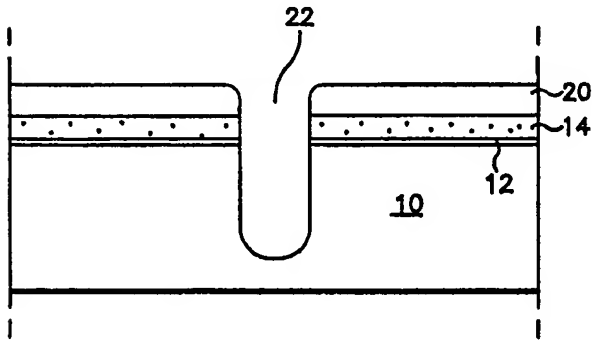


FIG. 2D

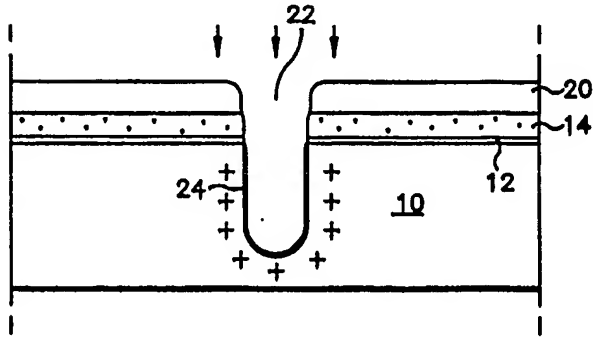


FIG. 2E

FIG. 2F

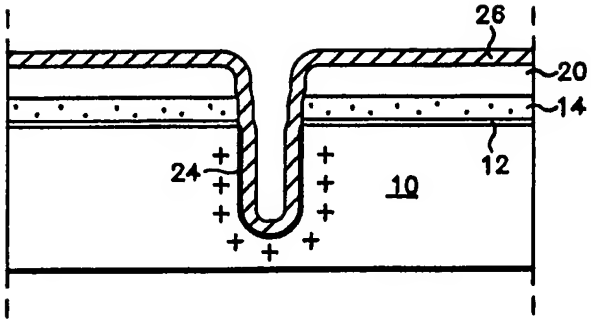


FIG. 2G

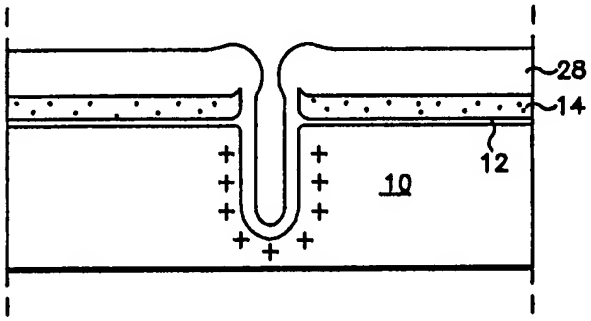


FIG. 2H

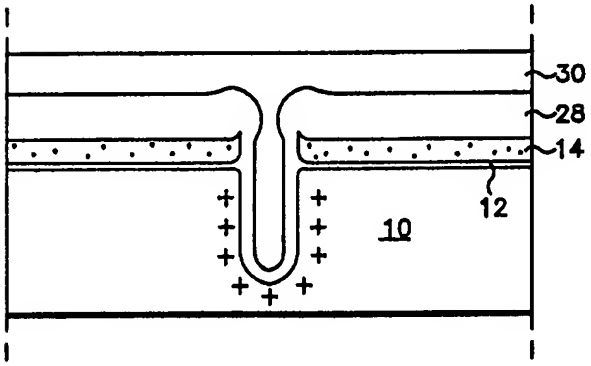
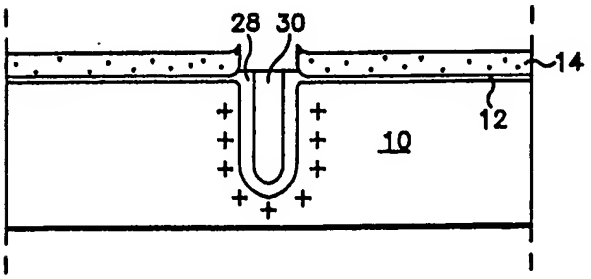


FIG. 2I



ELEMENT-ISOLATING PROCESS FOR A SEMICONDUCTOR DEVICE

The present invention relates to an element-isolating process for a semiconductor device, and particularly to a process for forming element-isolating regions by means of a trench structure.

Element-isolating regions of semiconductor devices play a role of providing electrical isolation between elements thereof. However the increase of density of semiconductor device makes the electrical isolation process very difficult. That is, VLSI (Very Large Scale Integrated Circuit) technology requires element-isolating regions in the 0.3μm - 0.4μm range, but current photo-etching techniques are not capable of overcoming a limit of 0.5μm. Therefore, a new process suitable for VLSI devices is in urgent demand. On the other hand, even if element-isolating regions having a trench width below 0.5μm were to realized, the bird's beak phenomenon, which is liable to occur in the oxidization process after the etching of the trench, can not be inhibited.

Preferred embodiments of the present invention aim to provide a process of forming element-isolating regions in a semiconductor device, the element-isolating regions being provided with a trench width below the trench width released by current photo-etching techniques.

Another aim is to provide an element-isolating process for a semiconductor device, being capable of filling the interior of a trench without the bird's beak phenomenon accompanied by an etching of the trench.

According to a first aspect of the present invention, there is provided an element-isolating process for a semiconductor device, comprising the steps of:

successively depositing a first insulating layer, a second insulating layer and a first conductive layer over a top surface of a semiconductor substrate of a first conduction type;

subjecting a selected portion of said first conductive layer, corresponding to an element-isolating region, to an etching process, and thereafter subjecting the remainder of said first conductive layer to a thermal oxidation process so as to form an oxidized first conductive layer;

subjecting selected portions of said second insulating layer and said first insulating layer to an etching process until a selected top surface of said substrate is exposed, by using said oxidized first conductive layer as a mask;

forming a trench through an etching process applied to the exposed top surface of said substrate;

forming a buffer insulating layer on an inner wall of said trench, and thereafter depositing a second conductive layer over a remainder of whole surface of said substrate and said inner wall of said trench;

filling an interior of said trench with an insulating material; and

carrying out an etch-back process until a selected top surface of said second insulating layer is sufficiently exposed, and thereafter, removing an exposed portion of said second insulating layer through an etching process.

Preferably, formation of a pattern by said etching process for said selected portion of said first conductive layer, said pattern corresponding to said element-isolating region, is preferably carried out at a dimension corresponding to the minimum dimension obtainable by photo-etching technique.

Preferably, the width of said trench is controlled by the thickness of said first conductive layer.

Preferably, said first conductive layer is a polycrystalline silicon.

Preferably, said first insulating layer is a silicon oxide layer.

Preferably, said second insulating layer is a silicon nitride layer.

Preferably, said buffer insulating layer is an oxide layer.

Preferably, said second conductive layer is a polycrystalline silicon.

Preferably, said filling process comprises the steps of:

subjecting said second conductive layer to a thermal oxidation process; and

depositing a third insulating layer over said whole surface to a thickness sufficient to completely fill said interior of said trench.

Preferably, said filling process comprises a step of thermally oxidizing said second conductive layer until said interior of said trench is completely filled.

Preferably, said filling process comprises the steps of:

subjecting said second conductive layer to a thermal oxidation;

depositing an undoped polycrystalline silicon over said whole surface of said substrate; and

thermally oxidizing said undoped polycrystalline silicon sufficiently to completely fill said interior of said trench.

According to another aspect, the invention provides an element isolating process for a semiconductor substrate, comprising the steps of forming a trench in a semiconductor substrate and filling the trench with an insulating material.

Such a process may further comprise any one or more of the features disclosed in the accompanying specification, claims, abstract and/or drawings, in any combination.

According to a further aspect of the present invention, there is provided an element-isolating process for a semiconductor device, the process

comprising the steps of: successively depositing a first insulating layer made of an oxide layer, a second insulating layer made of a nitride layer, and a first conductive layer made of a polycrystalline silicon layer, upon a semiconductor substrate of a first conduction type; etching a selected portion of the first conductive layer corresponding to an element-isolating region, and subjecting the remainder of the first conductive layer to a thermal oxidation; successively removing the second and first insulating layers by using the oxidized first conductive layer as a mask; and forming a trench by subjecting the exposed substrate to etching.

The process may further comprise the steps of: forming a buffer insulating layer on the inner wall of the trench to stabilize a surface contacted with the silicon substrate; then depositing a second conductive layer of polycrystalline silicon over the surface of the silicon substrate; and filling the interior of the trench with only an oxidized second conductive layer by adjusting the oxidation of the second conductive layer, or filling the interior of the trench with an insulating material other than a nitride layer after the oxidation of the second conductive layer.

The invention also extends to a semiconductor device manufactured by a process as above, according to any of the above aspects of the invention.

For a better understanding of the invention, and to show how the same may be carried into effect, reference will now be made, by way of example, to the accompanying diagrammatic drawings, in which:

Figure 1 is a sectional view showing one example of a semiconductor device produced in accordance with a process which embodies of the present invention; and

Figures 2A - 2I illustrate respective steps in one example of such a manufacturing process.

Figure 1 is a sectional view showing trench isolating regions. The illustrated semiconductor device includes: an isolating-trench 22 having a width smaller than that provided with current photo-etching techniques, the trench 22 being formed in a selected position of a semiconductor substrate 10 of a first conduction type 10; an oxidized polycrystalline silicon layer 28 positioned adjacent to the inner wall of the trench 22; an insulating material 30 filling the interior of the trench; and a gate oxide layer 12 formed upon the selected portion of the substrate and connected to the oxidized polycrystalline silicon layer 28.

Figures 2A - 2I illustrate one example of a manufacturing process for the semiconductor device of Figure 1. In Figures 1 and 2, like reference numerals denote like or corresponding parts.

As shown in Figure 2A, a pad oxide layer 12, a nitride layer 14 and a first polycrystalline silicon layer 16 are successively deposited on the silicon substrate 10 of the first conduction type in thicknesses of 200 - 500 Å, 500 - 1500 Å and 1000 - 1500 Å respectively. Then a photoresist is deposited on the polycrystalline silicon layer 16, and a photoresist pattern 18 is formed by a photo-etching process. Thus a given portion of the polycrystalline silicon layer 16, corresponding to an element-isolating region, is exposed. Then the

exposed polycrystalline silicon layer is etched. Here, the pattern width of the element-isolating region is 0.5 μm, which is the limit of the photo-etching method.

As shown in Figure 2B, the photoresist pattern 18 is removed, and then, the remainder of the first polycrystalline silicon layer 16 is subjected to a thermal oxidation, to form an oxidized polycrystalline silicon layer 20, the oxidized polycrystalline silicon layer 20 swelling upwardly and sidewardly. The amount of swelling caused by the thermal oxidation is about 500 Å. A distance **d** between the inner sides of the oxidized polycrystalline silicon 20 is about 0.4 μm, and is controlled by the thickness of the original first polycrystalline silicon layer 16.

As shown in Figure 2C, a dry etching is applied to an exposed portion of the nitride layer 14 and the oxide layer 12, to remove them through the oxidized polycrystalline silicon layer 20 which serves as the mask. Thus a selected surface of the semiconductor substrate is exposed. As shown in Figure 2D, the exposed portion of the silicon substrate 10 is vertically etched to a depth of 0.5 - 3 μm by employing the oxidized polycrystalline silicon layer 20 as a mask, thereby forming the trench 22.

As shown in Figure 2E, a thermal oxidation is performed on the inner surface of the trench 22 to form a buffer oxide layer 24, and then, first conduction type impurities are ion-implanted thereinto, thereby forming an ion-implanted region for a field- stop.

As shown in Figure 2F, a second polycrystalline silicon layer 26 of a given thickness is formed upon the whole surface of the semiconductor device

and inner wall of the trench. Then, as shown in Figure 2G, a thermal oxidation is applied to the second polycrystalline silicon layer 26, thereby forming an oxidized polysilicon layer 28 which swells upwardly and sidewardly.

As shown in Figure 2H, an insulating layer 30 is deposited over the whole surface of the substrate 10, sufficient to completely fill the interior of the trench, and is then flattened. In forming the insulating layer 30, a nitride layer should not be used, because the oxidized silicon layer 28 and the insulating layer 30 will be simultaneously etched back by employing the nitride layer 14 as an etch-stop layer in the following step.

As shown in Figure 2I, the oxidized polycrystalline silicon layer 28 and the insulating layer 30 are sufficiently etched until the surface of the nitride layer 14 is sufficiently exposed. Then, the nitride layer 14 is removed by receiving a wet etching, thereby completing the formation of the element-isolating region in the form of a trench.

In the above described embodiment of the present invention, the interior of the trench is occupied with an insulating layer other than a nitride layer as shown in Figure 2H. However, in another embodiment according to the present invention, instead of the nitride layer, undoped polycrystalline silicon occupies the interior of the trench, and then the undoped polycrystalline silicon is oxidized. In the illustrated embodiment, an insulating layer is deposited after oxidizing the second polycrystalline silicon layer as shown in Figure 2G. However, in still another embodiment of the present invention, the interior of the trench can be filled with only the second

polycrystalline silicon without additionally depositing a insulating layer, by adequate control of the oxidation of the second polycrystalline silicon layer.

According to the example of the present invention as described above, the width of the photoresist pattern is formed up to the limit-width of photo-etching technique, and then, by utilizing the volume expansion based on a thermal oxidation of the polycrystalline layer, finally an element-isolating region of 0.3 - 0.4 μm is achieved. Further, since a buffer oxide layer and a polycrystalline silicon layer are successively formed on the inner wall of the trench and thereafter a thermal oxidation is carried out on the polycrystalline silicon layer, a trench type element-isolating region, in which the occurrence of bird's beak phenomenon is suppressed, is formed. As a result, such embodiments of the present invention may greatly assist an increase in density of semiconductor devices.

While preferred embodiments of the invention have been particularly shown and described, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made without departing from the spirit and scope of the invention.

The reader's attention is directed to all papers and documents which are filed concurrently with or previous to this specification in connection with this application and which are open to public inspection with this specification, and the contents of all such papers and documents are incorporated herein by reference.

All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any

method or process so disclosed, may be combined in any combination, except combinations where at least some of such features and/or steps are mutually exclusive.

Each feature disclosed in this specification (including any accompanying claims, abstract and drawings), may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.

The invention is not restricted to the details of the foregoing embodiment(s). The invention extends to any novel one, or any novel combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

CLAIMS:

1. An element-isolating process for a semiconductor device, comprising the steps of:

successively depositing a first insulating layer, a second insulating layer and a first conductive layer over a top surface of a semiconductor substrate of a first conduction type;

subjecting a selected portion of said first conductive layer, corresponding to an element-isolating region, to an etching process, and thereafter subjecting the remainder of said first conductive layer to a thermal oxidation process so as to form an oxidized first conductive layer;

subjecting selected portions of said second insulating layer and said first insulating layer to an etching process until a selected top surface of said substrate is exposed, by using said oxidized first conductive layer as a mask;

forming a trench through an etching process applied to the exposed top surface of said substrate;

forming a buffer insulating layer on an inner wall of said trench, and thereafter depositing a second conductive layer over a remainder of whole surface of said substrate and said inner wall of said trench;

filling an interior of said trench with an insulating material; and

carrying out an etch-back process until a selected top surface of said second insulating layer is sufficiently exposed, and thereafter, removing an exposed portion of said second insulating layer through an etching process.

2. An element-isolating process for a semiconductor device as claimed in claim 1, wherein formation of a pattern by said etching process for said selected portion of said first conductive layer, said pattern corresponding to said element-isolating region, is preferably carried out at a dimension corresponding to the minimum dimension obtainable by photo-etching technique.

3. An element-isolating process for a semiconductor device as claimed in claim 1 or 2, wherein the width of said trench is controlled by the thickness of said first conductive layer.

4. An element-isolating process for a semiconductor device as claimed in any of claims 1 to 3, wherein said first conductive layer is a polycrystalline silicon.

5. An element-isolating process for a semiconductor device as claimed in any of the preceding claims, wherein said first insulating layer is a silicon oxide layer.

6. An element-isolating process for a semiconductor device as claimed in any of the preceding claims, wherein said second insulating layer is a silicon nitride layer.

7. An element-isolating process for a semiconductor device as claimed in any of the preceding claims, wherein said buffer insulating layer is an oxide layer.

8. An element-isolating process for a semiconductor device as claimed in any of the preceding claims, wherein said second conductive layer is a polycrystalline silicon.

9. An element-isolating process for a semiconductor device as claimed in any of the preceding claims, wherein said filling process comprises the steps of:

subjecting said second conductive layer to a thermal oxidation process;and

depositing a third insulating layer over said whole surface to a thickness sufficient to completely fill said interior of said trench.

10. An element-isolating process for a semiconductor device as claimed in any of claims 1 to 8, wherein said filling process comprises a step of thermally oxidizing said second conductive layer until said interior of said trench is completely filled.

11. An element-isolating process for a semiconductor device as claimed any of claims 1 to 8, wherein said filling process comprises the steps of:

subjecting said second conductive layer to a thermal oxidation;

depositing an undoped polycrystalline silicon over said whole surface of said substrate; and

thermally oxidizing said undoped polycrystalline silicon sufficiently to completely fill said interior of said trench.

12. An element isolating process for a semiconductor substrate, comprising the steps of forming a trench in a semiconductor substrate and filling the trench with an insulating material.

13. A process according to claim 12, further comprising any one or more of the features disclosed in the accompanying specification, claims, abstract and/or drawings, in any combination.

14. An element-isolating process for a semiconductor device, substantially as hereinbefore described with reference to the accompanying drawings.

15. A semiconductor device manufactured by a process according to any of the preceding claims.

Patents Act 1977
Examiner's report to the Comptroller under S tion 17 (The Search Report)

Application number 9114158.0

Relevant Technical fields

(i) UK Cl (Edition K) H1K (KGCC)

(ii) Int Cl (Edition 5) H01L

Search Examiner: C D STONE

Databases (see over)

(i) UK Patent Office

(ii)

Date of Search: 8 August 1991

Documents considered relevant following a search in respect of claims 1-12, 14, 15

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
X	GB A 2217909 MITSUBISHI DENKI	12
X	GB A 2148593 HITACHI	12
X	GB A 2148591 HITACHI	12
X	EP A2 0349107 SONY	12
X	EP A2 0178649 HITACHI	12
X	EP A1 0139371 TEKTRONIX	12
X	EP A2 0107902 FUJITSU	12
X	EP A2 0072966 I.B.M	12
X	EP A1 0020994 I.B.M	12
X	WO A1 87/04856 N.C.R	12

Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family, corresponding document.

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